REMARKS

Applicant would like to thank the Examiner for the thorough review of the present application. As discussed in detail below, the present claims include recitations that patentably distinguish the claimed invention over the cited references, taken individually or in combination. Based upon the following remarks, Applicant respectfully requests reconsideration of the present application and allowance of the pending claims.

Claim Status

Claims 2, 3, 5-21 are currently pending in the present application.

Claims 2, 3, 5-10, 12-14, 16 and 18-21 have been amended to overcome rejections, add clarity and particularly point out and distinctly claim the subject matter of the present invention.

Claim Rejections Under 35 U.S.C. § 112, Second Paragraph

Claims 2, 3 5-7 and 19-21 stand rejected under 35 U.S.C. § 112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter of the invention.

Claims 6 and 20 have been amended to address the issue related to lack of proper antecedent basis. Specifically, claims 6 and 20 have been amended such that the capacitor of the respective independent claims 2 and 3, further includes a first and a second electrode.

Claims 7 and 21 have been amended to address the issue related to lack of proper antecedent basis. Specifically, claims 7 and 21 have been amended such that the capacitor of the respective independent claims 2 and 3 further includes a dielectric layer.

Claims 2 and 3 have been amended to overcome the indefiniteness related to use of the phrase "formed in the same layer". The Examiner asserted that is was unclear as to what layer "the same layer" was referring to. Applicant has amended the wherein clause of claims 2 and 3 such that, "the capacitor and the first metal interconnection are formed in a substantially equivalent vertical plane of the semiconductor device." Applicant reasons that the previous intent of the term "formed in the same layer" was to claim that the capacitor and the first metal interconnect are formed in a substantially equivalent vertical plane of the semiconductor device. Support for this new language can be found in the specification at various instances, such as the abstract, which provides for "A method for fabricating a semiconductor device that forms a capacitor and metal interconnection in the same level." Further support for the new claim language is shown throughout the figure set of the present application, which depict the capacitor and the first metal interconnection formed in a substantially equivalent vertical plane of the semiconductor device. Applicant reasons that forming the capacitor and the metal interconnection "in the same level" is structurally equivalent to forming the capacitor and the first metal interconnection "in a substantially equivalent vertical plane of the semiconductor device". Additionally, Applicant believes that the present amended language in claims 2 and 3 provide more definiteness to the claim than either the phrase "the same layer" or "the same level".

Claim Rejections Under 35 U.S.C. § 102(b)

Claim 2 stands rejected under 35 U.S.C. § 102(b) as being anticipated by United States Patent No. 6,281,541, issued to Hu (hereinafter, the Hu patent). Applicant respectfully submits that this rejection is overcome by the following arguments and amendments made to claim 2.

The Hu Patent Does Not Teach or Suggest Forming a Capacitor in the Second Trench

Claim 2 of the present application specifically recites forming a capacitor in the second trench. As shown in Figure 1 of the present application the capacitor (172) is formed in the second trench (154). The capacitor includes a first electrode (160), a dielectric (165) and a second electrode (170), which are layered inside the bottom wall and the sidewall of the second

trench (154). The Applicant asserts that for the capacitor to be formed *in the second trench*, each component of the capacitor, specifically the first and second electrodes (160, 170) and the dielectric (165) must be disposed within the second trench (154).

The Hu patent teaches a semiconductor device including a capacitor (58). As noted in the Hu specification, at column 2, lines 51-53, the bottom plate of the electrode of the capacitor (58) is from metal plugs (30). Additionally, as noted in the Hu specification, at column 2, line 54, the capacitor (58) includes capacitor dielectric layer (36). The capacitor (58) also includes metal layer (52), which forms the upper electrode, as taught by the Hu specification at column 4, lines 4-5. Thus, the only elements of the capacitor that are taught to be formed in the second trench, identified by the Examiner as trench (35), are the dielectric layer (36) and the upper electrode/metal layer (52). The metal plugs (30), which form the bottom plate of the electrode are formed in the first trench (25) and, thus, not formed "in" the second trench (35). Therefore, since all of the elements of the capacitor taught in the Hu patent, specifically the bottom plate electrode/metal plugs (30), are not formed in the second trench, the Hu teachings are patentably distinguishable from the claim 2 invention.

The Hu Patent Does Not Teach or Suggest a Semiconductor Device in Which the Capacitor and the First Metal Interconnection are Formed in a Substantially Equivalent Vertical Plane.

Claim 2 has been amended to specifically require that the capacitor and the first metal interconnection be formed in a substantially equivalent vertical plane of the semiconductor device. In this regard, the capacitor and the first metal interconnect are formed in substantially the same layer or level of the semiconductor device. This is because the capacitor and the first metal interconnect are formed by a damascene process that selectively etches an insulation layer to form trenches to a depth defined by an etch blocking layer and then forming the capacitor and the first metal interconnect in the trenches. Thereby, limiting the number of processing steps required to form the semiconductor device of the present invention.

According the Examiner, the Hu patent teaches a semiconductor device in which the capacitor and the first metal interconnect reside in different vertical planes. According to the

Examiner, the first metal interconnect comprises the metal plug (30) and, according to the Hu specification, the capacitor (58) comprises the metal plug (30), the dielectric layer (36) and the metal layer (52). Thus, the first metal interconnect resides in a first vertical plane that comprises the depth of the metal plug (30). The capacitor resides in a second vertical plane that comprises the depth of the metal plug (30), the dielectric layer (36) and the metal layer (52). Thus, in the Hu patent the first metal interconnect and the capacitor reside in different vertical planes. Therefore, since the capacitor and the first metal interconnect are not formed in a substantially equivalent vertical plane, the Hu teachings are patentably distinguishable from the claim 2 invention.

Accordingly, Applicant respectfully requests reconsideration and withdrawal of the 35 U.S.C. § 102(b) rejection of claim 2. Claims 5-7 are believed allowable for at least the same reasons as presented above with respect to claim 2 by virtue of their dependence from claim 2.

Claim Rejections Under 35 U.S.C. § 103(a)

Claim 2-3, 5-7, 16-18 and 19-21 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over United States Patent No. 6,346,454, issued to Sung et al. (hereinafter the Sung patent) in view of the Hu patent. Applicant respectfully submits that this rejection is overcome by the following arguments.

Neither the Sung Patent or the Hu Patent Teach or Suggest Forming a Third Trench in the First Barrier Metal by Selectively Etching the First Metal Interconnection in the Capacitor Region and Forming a Capacitor in the Second and the Third Trenches

Independent claims 3 and 16 of the present invention specifically require forming three trenches. The third trench (156 of Fig. 4A) is formed in the first barrier metal by selectively etching the first metal or copper interconnection in the capacitor region. Once the third trench is formed, a capacitor is formed in both the second and third trenches.

Both the Sung patent and the Hu patent teach forming a two trenches but neither the Sung patent nor the Hu patent teach forming a third trench. The Examiner asserts that the Sung patent teaches the formation of a third trench. However, neither trench taught in the Sung patent, specifically trenches (57) and (56), is formed in the first barrier metal by selectively etching the first metal interconnection in the capacitor region and then forming a capacitor in the trench. The Sung patent teaches forming a capacitor in trench (56), however, this trench is not formed in the first barrier metal by selectively etching the first metal interconnection in the capacitor region. The Hu patent teaches forming a second trench (35), however this trench is not formed in the first barrier metal by selectively etching the first metal interconnection in the capacitor region. Since neither the Sung patent or the Ho patent teach or suggest forming a third trench and, moreover, forming a capacitor *in both* the second and third trenches, claims 3 and 16 of the present invention are distinguishable from the Sung and Ho patents and, thus can not be deemed to be unpatentable in combination because the two references lack a complete teaching of the claimed invention.

Accordingly, Applicant respectfully requests reconsideration and withdrawal of the 35 U.S.C. § 103(a) rejection of claims 3 and 16. Claims 17 and 18 and 19-21 are believed allowable for at least the same reasons as presented above with respect to claims 3 and 16 by virtue of their dependence from claims 3 and 16, respectively.

Neither the Sung Patent or the Hu Patent Teach or Suggest a Semiconductor Device in Which the Capacitor and the First Metal Interconnection are Formed in a Substantially Equivalent Vertical Plane.

Claim 2 has been amended to specifically require that the capacitor and the first metal interconnection be formed in a substantially equivalent vertical plane of the semiconductor device. In this regard, the capacitor and the first metal interconnect are formed in substantially the same layer or level of the semiconductor device. This is because the capacitor and the first metal interconnect are formed by a damascene process that selectively etches an insulation layer to form trenches to a depth defined by an etch blocking layer and then forming the capacitor and

the first metal interconnect in the trenches. Thereby, limiting the number of processing steps required to form the semiconductor device of the present invention.

As previously noted, the Hu patent lacks a teaching or suggestion of semiconductor device in which the capacitor and the first metal interconnection are formed in a substantially equivalent vertical plane.

The Sung patent teaches a semiconductor device in which the capacitor is formed in a first vertical plane and the first metal interconnection is formed in a second vertical plane that is different from the first vertical plane. The capacitor in the Sung patent is formed through the second dielectric layer (38), the etch stop layer (4) and the third dielectric layer (42). The metal interconnect layer (54), absent the contact (26) is formed by the metal line (27), which is formed through the third dielectric layer. Thus, the capacitor and the first metal interconnection are not formed in substantially the same vertical plane and, therefore, claim 2 of the present invention is distinguishable from the teachings of the Sung patent.

Accordingly, Applicant respectfully requests reconsideration and withdrawal of the 35 U.S.C. § 103(a) rejection of claim 2. Claims 5-7 are believed allowable for at least the same reasons as presented above with respect to claim 2 by virtue of their dependence from claim 2.

The Hu Patent Does Not Teach or Suggest Forming a Capacitor in the Second Trench

Claim 8 of the present application specifically recites forming a capacitor in the second trench. As shown in Figure 1 of the present application the capacitor (172) is formed in the second trench (154). The capacitor includes a first electrode (160), a dielectric (165) and a second electrode (170), which are layered inside the bottom wall and the sidewall of the second trench (154). The Applicant asserts that for the capacitor to be formed *in the second trench*, each component of the capacitor, specifically the first and second electrodes (160, 170) and the dielectric (165) must be disposed within the second trench (154).

The Hu patent teaches a semiconductor device including a capacitor (58). As noted in the Hu specification, at column 2, lines 51-53, the bottom plate of the electrode of the capacitor (58) is from metal plugs (30). Additionally, as noted in the Hu specification, at column 2, line 54, the capacitor (58) includes capacitor dielectric layer (36). The capacitor (58) also includes metal layer (52), which forms the upper electrode, as taught by the Hu specification at column 4, lines 4-5. Thus, the only elements of the capacitor that are taught to be formed in the second trench, identified by the Examiner as trench (35), are the dielectric layer (36) and the upper electrode/metal layer (52). The metal plugs (30), which form the bottom plate of the electrode are formed in the first trench (25) and, thus, not formed "in" the second trench (35). Therefore, since all of the elements of the capacitor taught in the Hu patent, specifically the bottom plate electrode/metal plugs (30), are not formed in the second trench, the Hu teachings are patentably distinguishable from the claim 8 invention.

Accordingly, Applicant respectfully requests reconsideration and withdrawal of the 35 U.S.C. § 103(a) rejection of claim 8. Claims 9-15 are believed allowable for at least the same reasons as presented above with respect to claim 8 by virtue of their dependence from claim 8.

Conclusion

Therefore, all objections and rejections having been addressed, it is respectfully submitted that the present application is in condition for allowance and a Notice to that effect is earnestly solicited. Should any questions remain unresolved, the Examiner is encouraged to contact the undersigned attorney for Applicants at the telephone number indicated below in order to expeditiously resolve any remaining issues.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 07-1337 and please credit any excess fees to such deposit account.

Respectfully submitted,

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